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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,428	11/02/2005	Pavel Peleska	2002P15038WOUS	5404

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/527,428	PELESKA ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12 and 14-21* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *0310 0509*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 8, 17-19 objected to because of the following informalities:

Referring to claim 8, "processing the external event" is understood to refer to "processing the external events".

Referring to claim 17, "a execution unit" is understood to refer to "an execution unit".

Further referring to claim 17, "the execution unit" does not agree with "each CPU comprising". It is understood to refer to "its execution unit".

Referring to claim 18, "the maximum" is understood to refer to "each CPU's maximum".

Referring to claim 19, "the completed" is understood to refer to "each CPU's completed".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Referring to claims 14 and 17, and subsequently claims 15, 16, 18-21, it is unclear how a CPU may comprise "a cache in the separate operating mode of an external event". For the purpose of examination, this is understood to refer to "a cache entry for an external event accessible in the separate operating mode".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 8-12, 14-21 rejected under 35 U.S.C. 102(b) as being anticipated by US 5384906 to Horst.

7. Referring to claim 8 Horst discloses a method for synchronizing external events supplied to a CPU, comprising:

storing the external events; retrieving the external events in a separate operating mode of the CPU; processing the external event by an execution unit of the CPU (From line 66 of column 3, "The process continues until all processors are stopped with each event counter having the same value. When this point is reached, the processors are then all stopped at the same point in the program. The wait signal is removed, the interrupt line to each processor is asserted, and all processors are restarted to handle the synchronizing event."); and

providing a maximum number of commands to execute prior to the CPU entering

the separate operating mode (From line 27 of column 7, "In this case, CPU-A executes code until event-4 is indicated in time at a point 250. When event-4 is detected, sync logic circuit 210 causes CPU-A to enter a wait state. Similarly, CPU-B continues running until event-5 is detected at a point 251 whereupon CPU-B enters a wait state. CPU-C executes code until event-6 is detected at a point 252 whereupon CPU-C enters a wait state. Since the number of events counted by CPU-A is less than the number of events counted by CPU-C, CPU-A resumes instruction execution at a point 253 until event-5 is detected at a point 254 whereupon CPU -A again enters a wait state. When it is ascertained that CPU-A still is behind CPU-C, instruction execution resumes at a point 255 until event-6 is detected at a point 256 whereupon CPU-A again enters a wait state. CPU-B undergoes a similar processing sequence. That is, when it is ascertained that the number of events counted for CPU-B is less than the maximum number of events counted by any of the three processors, CPU-B resumes instruction execution at a point 257 until the next event is detected at point 258 whereupon CPU-B enters a wait state, and so on. Since CPU-C counted the most events before the sync request was received, CPU-C remains in a wait state until the event counters for each of CPU-A, -B and -C are equal. When this occurs, the sync logic circuit 210 associated with each processor issues a synchronized external interrupt signal on line 238, releases the wait signal on line 196 and execution for each processor resumes at a common point 259." Wherein the number of instructions (point in code) executed is compared to the CPU that's farthest ahead (maximum).).

8. Referring to claim 9, Horst discloses the maximum number of commands is predetermined (From line 52 of column 3, "The processors typically are synchronized whenever an external interrupt occurs, although the system designer is free to define any synchronizing event. When an event requiring synchronization is detected by a sync logic circuit associated with the processor, the sync logic circuit generates a wait signal after the next processor event. A compare circuit associated with each processor tests the other event counters in the system and determines whether its associated processor is behind the others. If so, the sync logic circuit removes the wait signal until the next processor event.").

9. Referring to claim 10, 18, Horst discloses the maximum number of commands is specified by a command (From line 52 of column 3, "The processors typically are synchronized whenever an external interrupt occurs, although the system designer is free to define any synchronizing event. When an event requiring synchronization is detected by a sync logic circuit associated with the processor, the sync logic circuit generates a wait signal after the next processor event. A compare circuit associated with each processor tests the other event counters in the system and determines whether its associated processor is behind the others. If so, the sync logic circuit removes the wait signal until the next processor event.").

10. Referring to claim 11, Horst discloses comparing the number of instructions executed since a change to the separate operating mode with the maximum number of commands; and changing the CPU into the separate operating mode based on the comparison (From line 5 of column 4, "If no synchronizing event occurs before an event

counter reaches its maximum value, an overflow of the event counter forces resynchronization." Further, see from column 29 the section regarding "Modulo Cycle Counters".).

11. Referring to claim 12, Horst discloses the CPU remains in the separate operating mode by a controller until a second CPU has reached the separate operating mode (From line 52 of column 3, "The processors typically are synchronized whenever an external interrupt occurs, although the system designer is free to define any synchronizing event. When an event requiring synchronization is detected by a sync logic circuit associated with the processor, the sync logic circuit generates a wait signal after the next processor event. A compare circuit associated with each processor tests the other event counters in the system and determines whether its associated processor is behind the others. If so, the sync logic circuit removes the wait signal until the next processor event.").

12. Referring to claim 14, Horst discloses a CPU (From line 5 of column 26, "single CPU image", line 64 of column 26, "one logical processor".), comprising:

an execution unit (From line 24 of column 7, "a sync request (e.g., external interrupt) is received by CPUs-A, -B and -C, but where CPUs -A, -B and -C are executing different portions of code.");

a completed instruction counter element for counting a number of instructions executed by the execution unit since a change to a separate operating mode; a maximum instruction register element that can be specified by an instruction; a comparator element that compares the maximum instruction register element with the

completed instruction counter (From line 27 of column 7, "In this case, CPU-A executes code until event-4 is indicated in time at a point 250. When event-4 is detected, sync logic circuit 210 causes CPU-A to enter a wait state. Similarly, CPU-B continues running until event-5 is detected at a point 251 whereupon CPU-B enters a wait state. CPU-C executes code until event-6 is detected at a point 252 whereupon CPU-C enters a wait state. Since the number of events counted by CPU-A is less than the number of events counted by CPU-C, CPU-A resumes instruction execution at a point 253 until event-5 is detected at a point 254 whereupon CPU -A again enters a wait state. When it is ascertained that CPU-A still is behind CPU-C, instruction execution resumes at a point 255 until event-6 is detected at a point 256 whereupon CPU-A again enters a wait state. CPU-B undergoes a similar processing sequence. That is, when it is ascertained that the number of events counted for CPU-B is less than the maximum number of events counted by any of the three processors, CPU-B resumes instruction execution at a point 257 until the next event is detected at point 258 whereupon CPU-B enters a wait state, and so on. Since CPU-C counted the most events before the sync request was received, CPU-C remains in a wait state until the event counters for each of CPU-A, -B and -C are equal. When this occurs, the sync logic circuit 210 associated with each processor issues a synchronized external interrupt signal on line 238, releases the wait signal on line 196 and execution for each processor resumes at a common point 259." Wherein the number of instructions (point in code) executed is compared to the CPU that's farthest ahead (maximum).); and

a cache in the separate operating mode of an external event, the external event

retrieved for processing by the CPU while in the separate operating mode (From line 66 of column 3, "The process continues until all processors are stopped with each event counter having the same value. When this point is reached, the processors are then all stopped at the same point in the program. The wait signal is removed, the interrupt line to each processor is asserted, and all processors are restarted to handle the synchronizing event.").

13. Referring to claim 15, Horst discloses the maximum instruction register element has a predetermined value (See above cited line 27 of column 7 wherein the maximum value is determined prior.).

14. Referring to claim 16, 19, Horst discloses the completed instruction counter element is reset before leaving the separate operating mode (From line 48 of column 3, "Each processor has a counter, termed an event counter, which counts the number of processor events indicated since the last time the processors were synchronized.").

15. Referring to claim 17, Horst discloses a computer system, comprising: a first CPU; a second CPU; and a connection for a transmission of synchronization information of the separate operating modes between the first and second CPU (From line 24 of column 7, "a sync request (e.g., external interrupt) is received by CPUs-A, -B and -C, but where CPUs -A, -B and -C are executing different portions of code."),

wherein each CPU comprising: a execution unit (From line 24 of column 7, "a sync request (e.g., external interrupt) is received by CPUs-A, -B and -C, but where CPUs -A, -B and -C are executing different portions of code."),

a completed instruction counter element for counting a number instructions

executed by the execution unit since a change to a separate operating mode, a maximum instruction register element having a predetermined value, a comparator element that compares the maximum instruction register element with the completed instruction counter (From line 27 of column 7, "In this case, CPU-A executes code until event-4 is indicated in time at a point 250. When event-4 is detected, sync logic circuit 210 causes CPU-A to enter a wait state. Similarly, CPU-B continues running until event-5 is detected at a point 251 whereupon CPU-B enters a wait state. CPU-C executes code until event-6 is detected at a point 252 whereupon CPU-C enters a wait state. Since the number of events counted by CPU-A is less than the number of events counted by CPU-C, CPU-A resumes instruction execution at a point 253 until event-5 is detected at a point 254 whereupon CPU -A again enters a wait state. When it is ascertained that CPU-A still is behind CPU-C, instruction execution resumes at a point 255 until event-6 is detected at a point 256 whereupon CPU-A again enters a wait state. CPU-B undergoes a similar processing sequence. That is, when it is ascertained that the number of events counted for CPU-B is less than the maximum number of events counted by any of the three processors, CPU-B resumes instruction execution at a point 257 until the next event is detected at point 258 whereupon CPU-B enters a wait state, and so on. Since CPU-C counted the most events before the sync request was received, CPU-C remains in a wait state until the event counters for each of CPU-A, -B and -C are equal. When this occurs, the sync logic circuit 210 associated with each processor issues a synchronized external interrupt signal on line 238, releases the wait signal on line 196 and execution for each processor resumes at a common point 259."

Wherein the number of instructions (point in code) executed is compared to the CPU that's farthest ahead (maximum).), and

a cache in the separate operating mode of an external event, the external event retrieved for processing by the CPU while in the separate operating mode (From line 66 of column 3, "The process continues until all processors are stopped with each event counter having the same value. When this point is reached, the processors are then all stopped at the same point in the program. The wait signal is removed, the interrupt line to each processor is asserted, and all processors are restarted to handle the synchronizing event.").

16. Referring to claim 20, Horst discloses the first and second CPUs have different clock frequencies (From line 6 of column 31, "The three microprocessors will operate at different speeds because of the slight differences in the crystal oscillators in clock sources 17 and other factors. There will be a fastest processor, a slowest processor, and the other processor.").

17. Referring to claim 21, Horst discloses the first and second CPUs are different CPUs (From line 6 of column 31, "The three microprocessors will operate at different speeds because of the slight differences in the crystal oscillators in clock sources 17 and other factors. There will be a fastest processor, a slowest processor, and the other processor.").

Allowable Subject Matter

18. Claim 13 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Referring to claim 13, the prior art does not teach or fairly suggest in view of **all** the parent limitations, the CPU remains in the separate operating mode until the second CPU has reached an end of the separate operating mode.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Primary Examiner
Art Unit 2114

gc